DAY THIRTY SIX

Electronic Devices

Learning & Revision for the Day

- Energy Bands in Solids
- Semiconductors
- Semiconductor Diode
- Diode as a Rectifier
- Special Purpose Diodes
- Transistor
- Logic Gates

Energy Bands in Solids

According to band theory of solids, in a crystalline solid due to mutual interaction among valence electrons of neighbouring atoms, instead of sharp energy levels, energy bands are formed. Energy bands are of the following three types

(a) **Valence band** It is the energy band formed by a series of energy levels of valence electrons actually present. Ordinarily, valence band is completely filled and electrons in this band are unable to gain energy from external electric field. The highest energy level in a valence band at 0 K is called **fermi energy level**.

(b) **Conduction band** The energy band having just higher energy than the valence band is called conduction band. Electrons in conduction band are commonly called the free electrons.

(c) **Forbidden band** The energy gap between the valence band and the conduction band of a solid is called the **forbidden energy gap** E_g or forbidden band. Width of forbidden energy gap depends upon the nature of substance.

Semiconductors

- In semiconducting solids, the valence band is completely filled but conduction band is completely empty and the energy gap between them is small enough ($E_g < 3$ eV). At absolute zero temperature, it behaves as an **insulator**.
- A pure semiconductor, in which no impurity of any sort has been mixed, is called **intrinsic semiconductor**. Germanium ($E_g = 0.72$ eV) and silicon ($E_g = 1.1$ eV) are examples of intrinsic semiconductors.
- Electrical conductivity of pure semiconductor is very small. To increase the conductivity of a pure semiconducting material, it is doped with a controlled quantity (1 in 10^5 or 10^6) of suitable impurity. Such a doped semiconductor is called an **extrinsic semiconductor.**

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- The number of electrons reaching from valence band to conduction band, $n = AT^{3/2} e^{-E_g/2kT}$
  where, k = Boltzmann's constant, T = absolute temperature and A = atomic weight.

Superconductors

When few metals are cooled, then below a certain critical temperature, their electrical resistance suddenly becomes zero. In this state, these substances are called **superconductors** and this phenomena is called **superconductivity**. Mercury become superconductor at 4.2 K, lead at 7.25 K and niobium at 9.2 K.

Types of Extrinsic Semiconductor

1. *n*-type Semiconductor

To prepare an n-type semiconductor, a pentavalent impurity, e.g. P, As, Sb is used as a dopant with Si or Ge.

Such an impurity is called **donor impurity**, because each dopant atom provides one **free electron**.

In n-type semiconductor $n_e >> n_h$, i.e. electrons are majority charge carriers and the holes are minority charge carriers, such that $n_e \cdot n_h = n_i^2$. An n-type semiconductor is electrically neutral and is not negatively charged.

Conductivity, $\sigma \approx n_e \mu_e e$

2. *p*-type Semiconductor

To prepare a p-type semiconductor, a trivalent impurity, e.g. B, Al, In, Ga, etc., is used as a dopant with Si or Ge. Such an impurity is called **acceptor impurity** as each impurity atom wants to accept an electron from the crystal lattice. Thus, effectively each dopant atom provides a **hole**.

In p-type semiconductor $n_h >> n_e$, i.e. holes are majority charge carriers and electrons minority charge carriers, such that $n_h \cdot n_e = n_i^2$. A p-type semiconductor is electrically neutral and is not positively charged.

The number of free electrons in a semiconductor varies with temperature as $T^{3/2}$.

Conductivity, $\sigma \approx n_h \mu_h e$

Semiconductor Diode

A ***p*-*n* junction** is obtained by joining a small p-type crystal with a small n-type crystal without employing any other binding material in between them. Whenever a p-n junction is formed, electrons from n-region diffuse through the junction into p-region and the holes from p-region diffuse into n-region.

As a result of which neutrality of both n and p-regions is disturbed, and a thin layer of immobile negative charged ions appear near the junction in the p-crystal and a layer of positive ions appear near the junction in n-crystal.

This layer containing immobile ions is called **depletion layer**. The thickness of depletion layer is approximately of the order of 10^{-6} m.

The potential difference developed across the p-n junction due to diffusion of electrons and holes is called the **potential barrier** V_b (or emf of fictitious battery).

For germanium diode barrier potential is 0.3 V, but for Si diode, its value is 0.7 V. The barrier electric field developed due to it, is of the order of 10^5 Vm^{-1}.

Mobility of Charge Carriers

The mobility of a charge carrier is defined as the velocity gained by its per unit electric field, i.e. $\mu = V_d/E$.

NOTE Current in semiconductor is, $i = i_e + i_h = eA(n_e V_e + n_h V_h)$

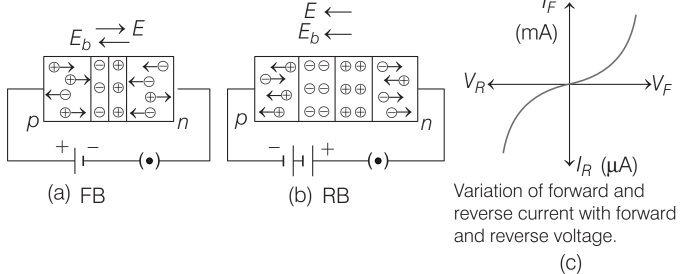
Conductivity, $\sigma = \frac{J}{E} = \frac{i}{AE} = e(n_e \mu_e + n_h \mu_h)$

(where, J = current density = nqV)

I-V Characteristics in Forward and Reverse Bias

When we join an external potential source, such that p-side of p-n junction is joined to positve of voltage source and n-side to negative of voltage source, the junction is said to be **forward biased** and applied electric field E opposes the barrier electric field E_b.

As a result, width of depletion layer is reduced and on applying a voltage $V > V_b$, a forward current begins to flow. Resistance offered by p-n junction in forward bias is small (about 10-50 Ω).



(a) FB (b) RB

Variation of forward and reverse current with forward and reverse voltage.
(c)

If connections of potential source are reversed [Fig. (b)], i.e. p-side is connected to negative terminal of battery and n-side to positive terminal, the junction is said to be **reverse biased** and in this case E and E_b, being in same direction, are added up. So, the depletion layer broadens and potential barrier is fortified.

Consequently, an extremely small leakage current flows across the junction due to minority charge carriers and junction resistance is extremely high ($\simeq 10^5$ Ω).

For a sufficiently high reverse bias voltage (25 V or even more), the reverse current suddenly increases. This voltage is called **Zener voltage** or **breakdown voltage** or **avalanche voltage**.

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Diode as a Rectifier

Junction diode allows current to pass only when it is forward biased. So, if an alternating voltage is applied across a diode, the current flows only in that part of the cycle, when the diode is forward biased.

This property is used to rectify alternating voltages and the circuit used for this purpose is called a rectifier, and the process is known as rectification.

There are two types of rectifier diode are given below

1. **Half Wave Rectifier** A rectifier, which rectifies only one-half of each AC input supply cycle, is called a **half wave rectifier.**

   A half wave rectifier gives discontinuous and pulsating DC output. As no output is obtained corresponding to alternate half cycles of the AC input supply, its efficiency is quite low.

2. **Full Wave Rectifier** A rectifier, which rectifies both halves of each AC input cycle is called a full wave rectifier.

   The output of a full wave rectifier is continuous, but pulsating in nature. However, it can be made smooth by using a filter circuit.

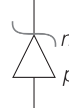
   As output is obtained corresponding to both the half cycles of the AC input supply, its efficiency is more than that of half wave rectifier.

NOTE • The ripple factor is defined as the ratio of rms value of AC component in the output of the rectifier to the DC component in the input.

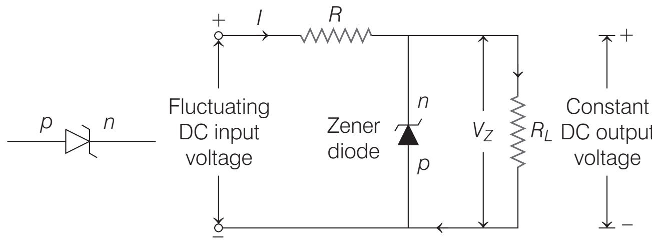
Special Purpose Diodes

Zener Diode

It is a highly doped *p-n* junction diode which is not damaged by high reverse current. It is always used in reverse bias in breakdown voltage region and is chiefly used as a voltage regulator.



- **Zener Diode as Voltage Regulator** The following circuit is used for stabilising voltage across a load R_L. The circuit consists of a series voltage-dropping resistance R and a Zener diode in parallel with the load R_L.

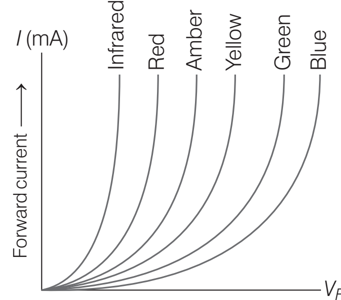


The Zener diode is selected with Zener voltage V_z equal to the voltage desired across the load.

Light Emitting Diode (LED)

It is a specially designed diode made of GaAsP, GaP, etc. When used in forward biased, it emits characteristic, almost monochromatic light. In reverse biased, it works like a normal diode.

- ***I-V* Characteristics of LED** LEDs are current dependent devices with its forward voltage drop (V_F) depending on the forward biased LED current. Light emitting diode *I-V* characteristics as given below



Photodiode

It is a special diode used in reverse bias which conducts only when light of suitable wavelengths is incident on the junction of diode. The energy of incident light photon must be greater than the band gap of semiconductor (i.e. $h\nu > E_g$). Materials used are Cds, Se, Zns, etc.

Solar Cell

It is a special *p-n* junction, in which one of the semiconductors is made extremely thin, so that solar radiation falling on it reaches junction of diode without any absorption. A solar cell directly converts, solar energy into electrical energy. Popularly used solar cells, Ni-cd, PbS cell, etc.

Transistor

A transistor is a combination of two *p-n* junctions joined in series. A junction transistor is known as **Bipolar Junction Transistor** (BJT). It is a three terminal device.

Transistors are of two types

(i) *n-p-n* transistor,

(ii) *p-n-p* transistor

A transistor has three regions

(i) An **emitter** (E), which is most heavily doped, and is of moderate size. It supplies large number of charge carriers, which are free electrons in an *n-p-n* transistor and holes in a *p-n-p* transistor.

(ii) A **base** (B), which is very lightly doped and is very thin (thickness $\approx 10^{-5}$m).

(iii) A **collector** (C), which is moderately doped and is thickest.

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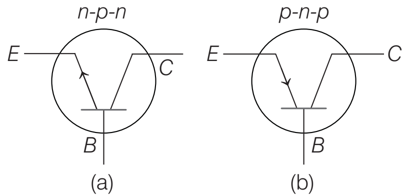
A transistor is symbolically represented as shown in figures.



Transistor Action

For proper functioning of a transistor, the **emitter-base junction is forward biased**, but the **collector-base junction** is **reverse biased.** In an *n-p-n* transistor, electrons flow from emitter towards the base and constitute a current I_E.

Due to larger reverse bias at base-collector junction, most of these electrons further pass into the collector, constituting a collector current I_C. But a small percentage of electrons (less than 5%) may combine with holes present in base. These electrons constitute a base current I_B. It is self evident, that

$$I_E = I_C + I_B.$$

Action of *p-n-p* transistor is also same, but with one difference that holes are moving from emitter to base and then to collector. A transistor can be connected in either of the following three configurations

(i) Common Emitter (CE) configuration

(ii) Common Base (CB) configuration

(iii) Common Collector (CC) configuration.

Generally, we prefer common emitter configuration, because power gain is maximum in this configuration.

Characteristics of a Transistor

In common emitter configuration, variation of current on the input side with input voltage (I_E *versus* V_{BE}) is known as the input characteristics, and the variation in the output current with output voltage (I_C *versus* V_{CE}) is known as output characteristics. From these characteristics, we obtain the values of following parameters

- Input resistance, $r_i = \left|\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$
- Output resistance, $r_o = \left|\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$
- AC current gain, $\beta = \left|\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$

  The current gain for common-emitter configuration β ranges from 20 to 200.
- Transconductance, $g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{\beta}{r_i}$
- A transistor can be used as an amplifier. The voltage gain of an amplifier will be given by

  $$A_V = \frac{V_o}{V_i} = \beta \cdot \frac{R_C}{R_B}$$

  where, R_C and R_B are net resistances in collector and base circuits, respectively.
- In common base configuration, AC current gain is defined as $\alpha = \left|\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CE} = \text{constant}}$
- Value of α is slightly less than 1. In fact, $0.95 \leq \alpha \leq 1$.
- Power gain $= \frac{\Delta P_o}{\Delta P_i} = \beta_{AC}^2 \times$ Resistance gain

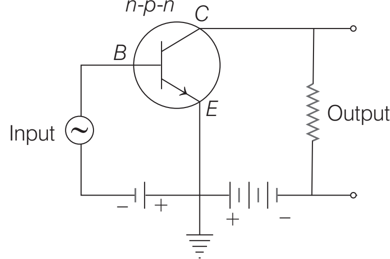
NOTE • Current gains α and β are correlated as

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{or} \quad \alpha = \frac{\beta}{1+\beta}$$

Transistor as an Amplifier

A transistor consisting of two *p-n* junctions, one forward biased and the other reverse biased can be used to amplify a weak signal. The forward biased junction has a low resistance path, whereas the reverse biased junction has a high resistance path. The weak input signal is applied across the forward biased junction, and the output signal is taken across the reverse biased junction.

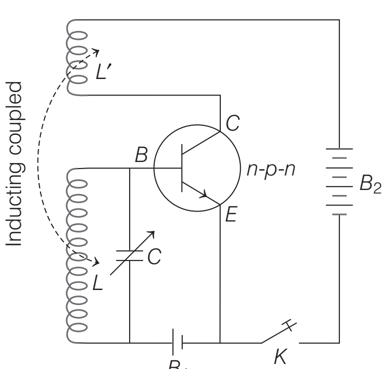
Since, the input and output currents are almost equal, the output signal appears with a much higher voltage. The transistor, thus acts as an amplifier. Common-emitter configuration of transistor amplifier is given below



Transistor as an Oscillator

An electronic oscillator is a device that generates electrical oscillations of constant amplitude and of a desired frequency, without any external input.

The circuit providing such oscillation, is known as a tank oscillator, is using positive feedback.



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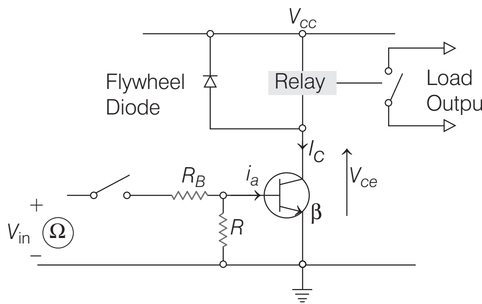
Some of the properties of the oscillator are

- Oscillator is using positive feedback.
- To work as an oscillator,
  $|A\beta| = 1; \beta \rightarrow$ feedback factor
- f = frequency of oscillation $= \frac{1}{2\pi} \times \frac{1}{\sqrt{LC}}$.

Transistor as a Switch

The circuit resembles that of the **Common-Emitter** circuit. The difference this time is that to operate the transistor as a switch the transistor needs to be turned either fully "OFF" (Cut-off) fully "ON" (Saturated). An ideal transistor switch would have an infinite resistance when turned 'OFF' resulting in zero current flow and zero resistance, when turned "ON", resulting in maximum current flow.

In practice, when turned "OFF", small leakage currents flow through the transistor and when fully "ON" the device has a low resistance value causing a small saturation voltage (V_{ce}) across it. In both the cut-off and saturation regions, the power dissipated by the transistor is at its minimum.



Logic Gates

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output.

At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels.

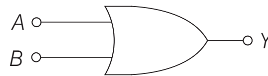
The logic **state** of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state in approximately zero volts (0V), while the high state is approximately five volts positive (+ 5V).

There are seven basic logic gates. AND, OR, NOT, XOR, NAND, NOR and XNOR.

The basic logic gates are of three types

The OR Gate

The OR gate is a davice has two or more inputs and one output. this devices combines two inputs to give one output. The logic symbol of OR gate is



The Boolean expression for OR gate is $Y = A + B$

This indicates Y equals A OR B.

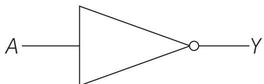
Truth table for OR gate ($Y = A + B$)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

The output of an OR gate assumes 1 if one of more inputs assume 1. The output is high when either of inputs A or B is high, but not if both A and B are high.

The AND Gate

The AND gate a device has also two or more inputs and one output. The logic symbol of AND gate is



The logic symbol of AND gate is given as under. The Boolean expression for AND gate is $Y = A \cdot B$, this indicates Y equals to A AND B.

Truth table for AND gate ($Y = A \cdot B$)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The output of an AND gate is 1 only, when all the inputs assume 1.

The NOT Gate

The NOT gate is a device which has only one input and only one output. The logic symbol of NOT gate is as shown in figure.

A ▷o Y

The Boolean expression for NOT gate is

$$Y = \overline{A},$$

which indicates Y equals NOT A.

Truth Table for NOT gate ($Y = \overline{A}$)

A	Y
0	1
1	0

The output of a NOT gate assumes 1, if input is 0 and *vice-versa.*

These basic gates (OR, AND and NOT) can be combined in various ways to provide large number of complicated digital circuits.

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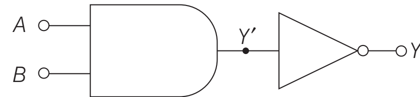
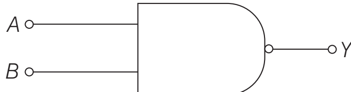
Combination of Logic Gates

1. NAND Gate

In this type of gate, the output of AND gate is fed to input of a NOT gate and final output is obtained at output of NOT gate.



The logic symbol of NAND gate is shown as



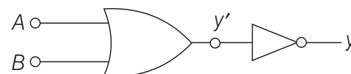
The Boolean expression of NAND gate is $Y = \overline{A \cdot B}$, which indicates A and B are negated.

Truth table for NAND gate

A	*B*	*Y′*	*Y*
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

2. NOR Gate

In this type of gate, the output of OR gate is fed to input of the NOT gate and final output is obtained at output of the NOT gate.



The logic symbol of NOR gate is shown as

A
B
$y = \overline{A + B}$

The Boolean expression for NOR gate is $Y = \overline{A + B}$, which indicates that 'A OR B are negated'

Truth table for NOR gate

A	*B*	*Y′*	*Y*
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

NOTE

- NAND and NOR gates are known as universal gate.
- The Boolean expressions obey the commutative law, associative law as well as distributive law.

Commutative law

(i) $A + B = B + A$ (ii) $A \cdot B = B \cdot A$

Associative law

(iii) $A + (B + C) = (A + B) + C$ (iv) $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

Distributive law

(v) $A \cdot (B + C) = A \cdot B + A \cdot C$ (vi) $A + \overline{A} \cdot B = A + B$

(vii) $A + A \cdot B = A$ (viii) $A \cdot (A + B) = A$

(ix) $A \cdot (\overline{A} + B) = A \cdot B$ (x) $\overline{A \cdot B} = \overline{A} + \overline{B}$

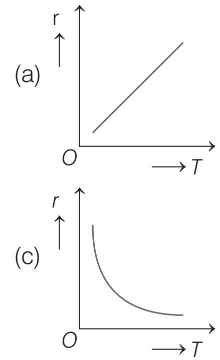
DAY PRACTICE SESSION 1

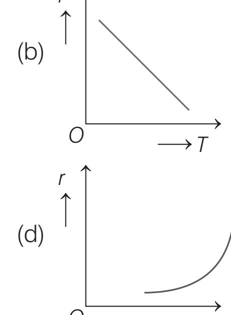
FOUNDATION QUESTIONS EXERCISE

1 The device that can act as a complete electronic circuit is ➜ CBSE AIPMT 2010

(a) junction diode (b) integrated circuit
(c) junction transistor (d) Zener diode

2 The temperature (T) dependence of resistivity (ρ) of a semiconductor is represented by





3 Which one of the following statement is false? ➜ CBSE AIPMT 2011

(a) Pure Si doped with trivalent impurities gives a *p*-type semiconductor
(b) Majority carriers in a *n*-type semiconductor are holes
(c) Minority carriers in a *p*-type semiconductor are electrons
(d) The resistance of intrinsic semiconductor decreases with increase of temperature

4 If a small amount of antimony is added to germanium crystal, ➜ CBSE AIPMT 2011

(a) the antimony becomes an acceptor atom
(b) there will be more free electrons than holes in the semiconductor
(c) its resistance is increased
(d) its capacitance is increased

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5 The conductivity of a semiconductor increases with increase in temperature because

(a) number density of free current carriers increase
(b) relaxation time increases
(c) both number density of carriers and relaxation time increase
(d) number density of current carriers increase, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density

6 In a *n*-type semiconductor, which of the following statement is true? ➞NEET 2013

(a) Electrons are majority carriers and trivalent atoms are dopants
(b) Electrons are minority carriers and pentavalent atoms are dopants
(c) Holes are minority carriers and pentavalent atoms are dopants
(d) Holes are majority carriers and trivalent atoms are dopants
(d) it becomes a *p*-type semiconductor

7 A specimen of silicon is to be made *p*-type semiconductor. For this one atom of indium, on an average, is doped in 5×10^7 silicon atoms. If the number density of silicon is 5×10^{28} atoms/m^2, then the number of acceptor atoms per cm^3 will be

(a) 2.5×10^{30} (b) 1.0×10^{13}
(c) 1.0×10^{15} (d) 2.5×10^{36}

8 The resistivity of an *n*-type extrinsic semiconductor is 0.25 Ω-m. If the electron mobility is 8.25 m^2/V-s, then the concentration of donor atoms will be (in m^{-3})

(a) 3.0×10^{16} (b) 3.0×10^{17} (c) 3.0×10^{18} (d) 3.0×10^{19}

9 The number of densities of electrons and holes in pure silicon at 27°C are equal and its value is 1.5×10^{16} m^{-3}. On doping with indium, the hole density increases to 4.5×10^{27} m^{-3}. The electron density in doped silicon will be

(a) 50×10^9 m^{-3} (b) 5×10^9 m^{-3}
(c) 10^8 m^{-3} (d) 10^7 m^{-3}

10 In *n*-type germanium, the mobility of electrons is 3900 cm^2/ Vs and their conductivity is 5 mho / cm. If the cotter contribution is negligible, then impurity concentration will be

(a) 8×10^{15} per cm^3 (b) 9.25×10^{14} per cm^3
(c) 6×10^{13} per cm^3 (d) 9×10^{13} per cm^3

11 The ratio of electron and hole currents in a semiconductor is $\frac{5}{4}$ and the ratio of drift velocities of electrons and holes is $\frac{7}{4}$, then the ratio of concentrations of electrons and holes will be

(a) $\frac{25}{49}$ (b) $\frac{49}{25}$ (c) $\frac{7}{5}$ (d) $\frac{5}{7}$

12 The contribution in the total current flowing through a semiconductor due to electrons and holes are $\frac{3}{4}$ and $\frac{1}{4}$. If the drift velocity of the electron is $\frac{5}{2}$ times that of holes at this temperature, then the ratio of concentration of electrons and holes is

(a) 6 : 5 (b) 5 : 6 (c) 3 : 2 (d) 2 : 3

13 Depletion layer contains

(a) Only immobile negative and positive ions
(b) Only free charge carrier
(c) Both free carrier and immobile ions
(d) None of the above

14 In an unbiased *p*-*n* junction, holes diffuse from the *p*-region to *n*-region because

(a) free electrons in the *n*-region attract them
(b) they move across the junction by the potential difference
(c) hole concentration in *p*-region is more as compared to *n*-region
(d) All of the above

15 The barrier potential of a *p*-*n* junction depends on

I. Type of semiconductor material
II. Amount of doping
III. Temperature

Which one of the following is correct? ➞CBSE AIPMT 2014

(a) I and II (b) Only II (c) II and III (d) I, II and III

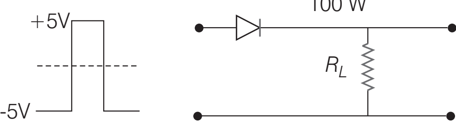
16 In forward biasing of the *p*-*n* junction ➞CBSE AIPMT 2011

(a) the positive terminal of the battery is connected to *n*-side and the depletion region becomes thin
(b) the positive terminal of the battery is connected to *n*-side and the depletion region becomes thick
(c) the positive terminal of the battery is connected to *p*-side and the deplection region become thin
(d) the positive terminal of the battery is connected to *p*-side and the depletion region becomes thick

17 Which one of the following represents forward bias diode? ➞NEET 2017

(a) 0V —▷|— R — −2 V
(b) −4V —▷|— R — −3 V
(c) −2V —▷|— R — +2 V
(d) 3V —▷|— R — 5 V

18 If in a *p*-*n* junction, a square input signal of 10 V is applied, as shown, ➞CBSE AIPMT 2015



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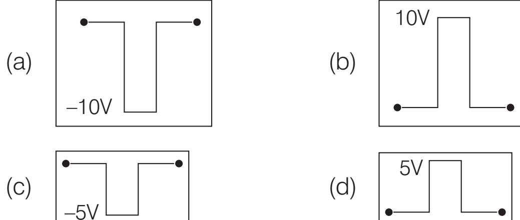
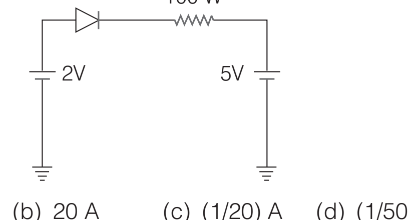
then the output across R_L will be

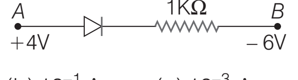


19 Current through the ideal diode as shown in figure, is



(a) zero (b) 20 A (c) (1/20) A (d) (1/50)A

20 Consider the junction diode as ideal. The value of current flowing through *AB* is ➞ NEET 2016



(a) 10^{-2} A (b) 10^{-1} A (c) 10^{-3} A (d) 0 A

21 LED has a voltage drop of 2 V across it, and passes a current of 10 mA. When it operates with a 6 V battery through a limiting resistor *R*. The value of *R* is

(a) 40 kΩ (b) 4 kΩ (c) 200 Ω (d) 400 Ω

22 The electrical conductivity of semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap (in eV) for the semiconductor is

(a) 0.9 (b) 0.7 (c) 0.5 (d) 1.1

23 A *p-n* photodiode is fabricated from a semiconductor with a band gap of 2.5 eV. It can detect a signal of wavelength ➞ CBSE AIPMT 2009

(a) 6000 Å (b) 4000 nm (c) 6000 nm (d) 4000 Å

24 In a transistor, the base is ➞ AFMC 2012

(a) an insulator
(b) a conductor of low resistance
(c) a conductor of high resistance
(d) an extrinsic semiconductor

25 The minimum potential difference between the base and emitter required to switch a silicon transistor ON, is approximately

(a) 1 V (b) 3 V (c) 5 V (d) 4.2 V

26 In a common base transistor circuit $I_C = 9.7\ \mu A$, $I_B = 0.03\ \mu A$, then current gain, $\alpha =$

(a) 0.97 (b) 0.097
(c) 95 (d) 500

27 In a common emitter amplifier, the output resistance is 5000 Ω and the input resistance is 2000 Ω. If the peak value of the signal voltage is 10 mV and $\beta = 50$, then the peak value of the output voltage is

(a) 1.25 V (b) 125 V
(c) 5×10^{-6} V (d) 2.5×10^{-4} V

28 The input and output resistances in a common base amplifier circuit are 400 Ω and 400 k Ω. If the current gain α is 0.98 and emitter current is 2 mA, then the base current is

(a) 0.02 mA (b) 0.08 mA (c) 0.05 mA (d) 0.04 mA

29 A *p-n-p* transistor is used in common emitter mode in an amplifier circuit. A charge of 40 μA in the base current brings a charge of 2 mA in collector current and of 0.04 V in base emitter voltage. The base current amplification factor is

(a) 5 (b) 50 (c) 500 (d) 0.5

30 The input resistance of a CE amplifier is 333 Ω and the load resistance is 5 kΩ. A change of base current by 15 μA a result in the change of collector current by 1 mA. The voltage gain of the amplifier is

(a) 550 (b) 51 (c) 101 (d) 1001

31 A common emitter amplifier has a voltage gain of 50, an input impedance of 100 Ω and an output impedance of 200 Ω. The power gain of the amplifier is ➞ CBSE AIPMT 2010

(a) 500 (b) 1000 (c) 1250 (d) 50

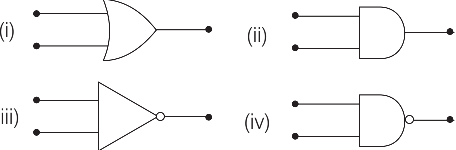
32 For CE transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 4 V. If the current amplification factor of the transistor is 100 and the base resistance is I kΩ, then the input signal voltage is ➞ NEET 2016

(a) 10 mV (b) 20 mV (c) 30 mV (d) 15 mV

33 A transistor is operated in common-emitter configuration at $V_C = 2$ volt such that a change in the base current from 100 μA to 200 μA produces a change in the collector current from 5 mA to 10 mA. The current gain is ➞ CBSE AIPMT 2009

(a) 75 (b) 100 (c) 150 (d) 50

34 Symbolic representation of four logic gates are shown as ➞ CBSE AIPMT 2011



Pick out which ones are for AND, NAND and NOT gates, respectively.

(a) (iii), (ii) and (i) (b) (iii), (ii) and (iv)
(c) (ii), (iv) and (iii) (d) (ii), (iii) and (iv)

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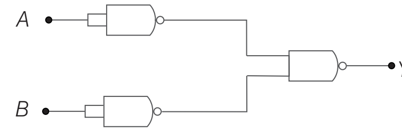
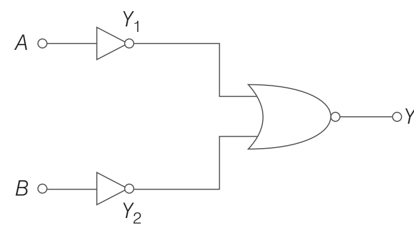
35 The combination of the gates shown in the figure below produces



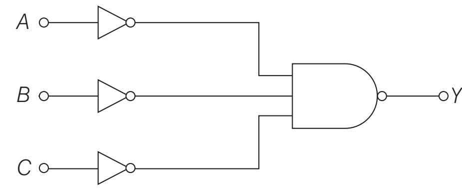
(a) NOR gate (b) OR gate
(c) AND gate (d) XOR gate

36 Which logic gate is represented by the following combination of logic gates? ➞ AIPMT 2015



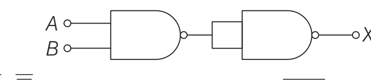
(a) OR (b) NAND (c) AND (d) NOR

37 A proper combination of 3 NOT and 1 AND gates is shown. If $A = 0$, $B = 1$ and $C = 1$, then the output of this combination is



(a) 1 (b) zero
(c) not predictable (d) None of these

38 The output (X) of the logic circuit shown in figure will be ➞ NEET 2013



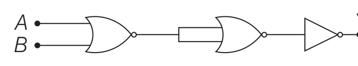
(a) $X = \overline{\overline{A}} \cdot \overline{\overline{B}}$ (b) $X = \overline{A \cdot B}$

(c) $X = A \cdot B$ (d) $X = \overline{A + B}$

39 Digital circuit can be made by repetitive use of this gate

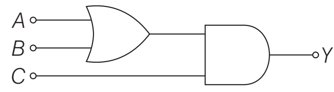
(a) AND (b) OR
(c) NOT (d) NAND

40 The given electrical network is equivalent to ➞ NEET 2017



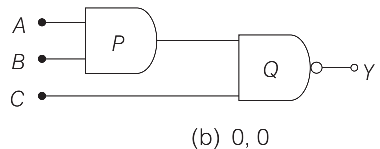
(a) AND gate (b) OR gate
(c) NOR gate (d) NOT gate

41 To get output 1 for the following circuit, the correct choice for the input is ➞ NEET 2016



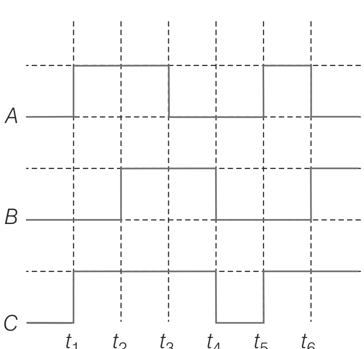
(a) $A = 1, B = 0, C = 0$ (b) $A = 1, B = 1, C = 0$
(c) $A = 1, B = 0, C = 1$ (d) $A = 0, B = 1, C = 0$

42 What is the output Y in the following circuit, when all the three inputs A, B, C are first 0 and then 1? ➞ NEET 2016



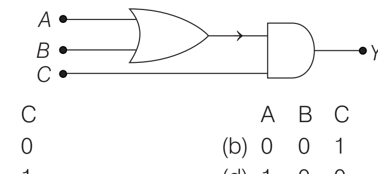
(a) 0, 1 (b) 0, 0
(c) 1, 0 (d) 1, 1

43 The figure shows a logic circuit with two inputs A and B, and the output C. The voltage waveforms across A, B and C are as given. The logic circuit gate is ➞ CBSE AIPMT 2012



(a) OR gate (b) NOR gate
(c) AND gate (d) NAND gate

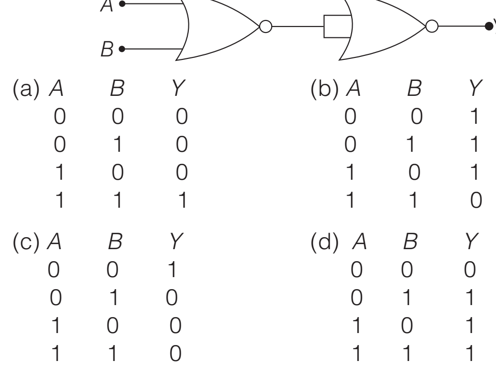
44 To get an output $Y = 1$ from the circuit shown below, the input must be ➞ CBSE AIPMT 2010



	A	B	C
(a)	0	1	0
(c)	1	0	1

	A	B	C
(b)	0	0	1
(d)	1	0	0

45 In the following circuit, the output Y for all possible inputs A and B is expressed by the truth table



(a)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(c)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(d)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

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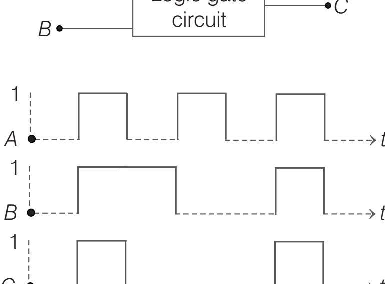
DAY PRACTICE SESSION 2

PROGRESSIVE QUESTIONS EXERCISE

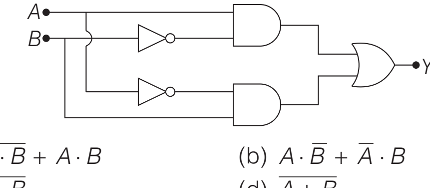
1 The following figure shows a logic gate circuit with two inputs A and B, and the output C. The voltage waveform of A, B and C are as shown below



The logic circuit gate is

(a) AND gate (b) NAND gate
(c) NOR gate (d) OR gate

2 In the combination of the following gates the output Y can be written in terms of inputs A and B as ➞NEET 2018

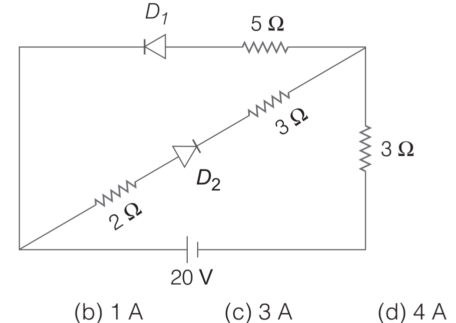


(a) $\overline{A \cdot B} + A \cdot B$ (b) $A \cdot \overline{B} + \overline{A} \cdot B$
(c) $\overline{A \cdot B}$ (d) $\overline{A + B}$

3 In a p-n junction diode, change in temperature due to heating

(a) does not affect resistance of p-n junction
(b) affects only forward resistance
(c) affects only reverse resistance
(d) affects the overall V-I characteristics of p-n junction

4 In the given circuit, all diodes are ideal. The current through battery is



(a) 2 A (b) 1 A (c) 3 A (d) 4 A

5 How many gates are required to design $P = X + \overline{X}Y$?

(a) 1 (b) 2 (c) 3 (d) 4

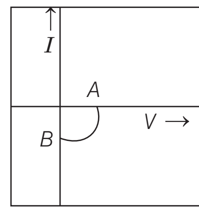
6 Assume that the number of hole-electron pairs in an intrinsic semiconductor is proportional to $e^{-\Delta E/2kT}$. Here, ΔE = energy gap and $k = 8.62 \times 10^{-5}$ eV/K. The energy gap for silicon is 1.1 eV. The ratio of electron-hole pairs at 300 K and 400 K, is

(a) $e^{-5.31}$ (b) e^{+5}
(c) e (d) e^{+3}

7 A potential difference of 2.5 V is applied across the faces of a germanium crystal plate. The face area of the crystal is 1cm^2 and its thickness is 1.0 mm. The free electron concentration in germanium is $2 \times 10^{19}\ \text{m}^{-3}$, and the electron and hole mobilities are $0.33\ \text{m}^2/\text{Vs}$ and $0.17\ \text{m}^2/\text{Vs}$, respectively. The current across the plate will be

(a) 0.2 A (b) 0.4 A
(c) 0.6 A (d) 0.8 A

8 The given graph represents V-I characteristic for a semiconductor device. Which of the following statement is correct? ➞CBSE AIPMT 2014



(a) It is V-I characteristic for solar cell, where point A represents open circuit voltage and point B short circuit current.
(b) It is for a solar cell and points A and B, represent open circuit voltage and current, respectively.
(c) It is for a photodiode and points A and B, represent open circuit voltage and current, respectively.
(d) It is for a LED and points A and B, represent open circuit voltage and short circuit current respectively.

9 C and Si both have same lattice structure, having 4 bonding electrons in each. However, C is insulator, whereas Si is intrinsic semiconductor. This is because ➞CBSE AIPMT 2012

(a) in case of C, the valence band is not completely filled at absolute zero temperature
(b) in case of C, the conduction band is partly filled even at absolute zero temperature
(c) the four bonding electrons in the case of C lie in the second orbit, whereas in the case of Si, they lie in the third
(d) the four bonding electrons in the case of C lie in the third orbit, whereas for Si, they lie in the fourth orbit

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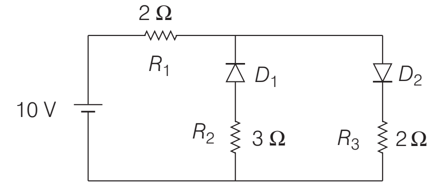
10 The given circuit has two ideal diodes connected as shown in the figure below. The current flowing through the resistance R_1 will be → NEET 2016

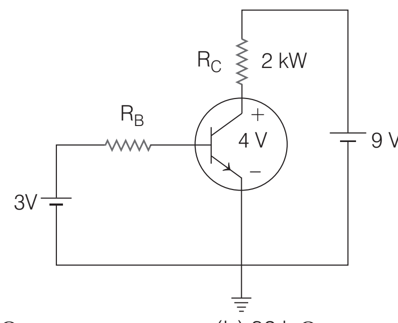


(a) 2.5 A (b) 10.0 A (c) 1.43 A (d) 3.13 A

11 The input signal given to a *CE* amplifier having a voltage gain of 150 is $V_i = 2\cos\left(15t + \frac{\pi}{3}\right)$. The corresponding output signal will be → CBSE AIPMT 2015

(a) $300\cos\left(15t + \frac{\pi}{3}\right)$ (b) $75\cos\left(15t + \frac{2\pi}{3}\right)$
(c) $2\cos\left(15t + \frac{5\pi}{3}\right)$ (d) $300\cos\left(15t + \frac{4\pi}{3}\right)$

12 The base resistance R_B in the circuit, is (given $h_{FE} = 90$)



(a) 10 k Ω (b) 82 k Ω
(c) 100 k Ω (d) 0.82 k Ω

13 In a Common Emitter (CE) amplifier having a voltage gain *G*, the transistor used has transconductance 0.03 mho and current gain 25. If the above transistor is replaced with another one with transconductance 0.02 mho and current gain 20, the voltage gain will → NEET 2013

(a) $\frac{2}{3}G$ (b) 1.5 G
(c) $\frac{1}{3}G$ (d) $\frac{5}{4}G$

14 In a CE transistor amplifier, the audio signal voltage across the collector resistance of 2 k Ω is 2 V. If the base resistance is 1k Ω and the current amplification of the transistor is 100, the input signal voltage is → CBSE AIPMT 2012

(a) 0.1 V (b) 1.0 V
(c) 1 mV (d) 10 mV

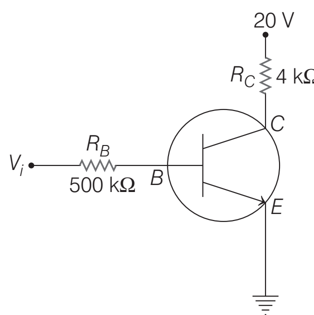
15 In a common emitter transistor amplifier, the audio signal voltage across the collector is 3 V. The resistance of collector is 3 kΩ. If current gain is 100 and the base resistance is 2 kΩ, the voltage and power gain of the amplifier is → NEET 2017

(a) 200 and 1000 (b) 15 and 200
(c) 150 and 15000 (d) 20 and 2000

16 A *n-p-n* transistor is connected in common emitter configuration in a given amplifier. A load resistance of 800 Ω is connected in the collector circuit and the voltage drop across it is 0.8V. If the current amplification factor is 0.96 and the input resistance of the circuits is 192 Ω, the voltage gain and the power gain of the amplifier will respectively be → NEET 2016

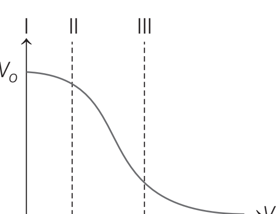
(a) 3.69, 3.84 (b) 4, 4
(c) 4, 3.69 (d) 4, 3.84

17 In the circuit shown in the figure, the input voltage V_i is 20 V, $V_{BE} = 0$ and $V_{CE} = 0$. The values of I_B, I_C and β are given by → NEET 2018



(a) $I_B = 20\,\mu A$, $I_C = 5$ mA, $\beta = 250$
(b) $I_B = 25\,\mu A$, $I_C = 5$ mA, $\beta = 200$
(c) $I_B = 40\,\mu A$, $I_C = 10$ mA, $\beta = 250$
(d) $I_B = 40\,\mu A$, $I_C = 5$ mA, $\beta = 125$

18 Transfer characteristic [output voltage (V_o) *vs* input voltage (V_i)] for a base biased transistor in CE configuration is as shown in the figure. For using transistor as a switch, it is used → CBSE AIPMT 2012



(a) in region III
(b) both in region (I) and (III)
(c) in region II
(d) in region I

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ANSWERS

SESSION 1	**1** (b)	**2** (c)	**3** (b)	**4** (b)	**5** (d)	**6** (c)	**7** (c)	**8** (c)	**9** (b)	**10** (a)
	11 (d)	**12** (a)	**13** (a)	**14** (c)	**15** (d)	**16** (c)	**17** (a)	**18** (d)	**19** (a)	**20** (a)
	21 (d)	**22** (c)	**23** (d)	**24** (b)	**25** (a)	**26** (a)	**27** (a)	**28** (d)	**29** (b)	**30** (d)
	31 (c)	**32** (b)	**33** (d)	**34** (c)	**35** (b)	**36** (c)	**37** (a)	**38** (c)	**39** (d)	**40** (c)
	41 (c)	**42** (c)	**43** (a)	**44** (c)	**45** (d)					
SESSION 2	**1** (a)	**2** (b)	**3** (d)	**4** (a)	**5** (a)	**6** (a)	**7** (b)	**8** (a)	**9** (c)	**10** (a)
	11 (d)	**12** (b)	**13** (a)	**14** (d)	**15** (c)	**16** (d)	**17** (d)	**18** (b)		

Hints and Explanations

SESSION 1

1 Integrated circuits are miniature electronic circuit produced within a single crystal of a semiconductor such as silicon. They contain a million or so transistors and resistors or capacitors. They are widely used in memory circuits, micro computers, pocket calculators and electronic watches on account of their low cost and bulk, reliability into specific regions of the semiconductor crystals.

2 The resistivity of a semiconductor decreases with increase in temperature exponentially.

3 *p*-type semiconductor are obtained by adding a small amount of trivalent impurity to a pure sample of semiconductor (Ge).
Majority charge carriers — holes
Minority charge carriers — electrons
In *n*-type semiconductor,
Majority charge carriers—electrons
Minority charge carriers —holes
The resistance of intrinsic semiconductors decreases with increase of temperature.

4 When a small amount of antimony is added to germanium crystal, the crystal becomes *n*-type semiconductor because antimony is a pentavalent substrate. It excess free electrons.

5 As temperature increases, increase in number density of current carriers is dominant. Hence, conductivity increases.

6 The *n*-type semiconductor can be produced by doping an impurity atom of valence 5, i.e. pentavalent atoms, i.e. phosphorus.

7 Number of acceptor atoms/cm^3

$$= \frac{5\times 10^{22}}{5\times 10^{7}} = 1\times 10^{15}\ \text{cm}^{-3}$$

8 $$\rho = \frac{1}{ne\mu_e} \text{ or } n = \frac{1}{\rho e\mu_e}$$

$$= \frac{1}{0.25\times 1.6\times 10^{-19}\times 8.25}$$

$$= 3.0\times 10^{18}\ \text{m}^{-3}$$

9 $$n_i^2 = n_e n_h$$

$$\therefore\ n_e = \frac{n_i^2}{n_h} = \frac{2.25\times 10^{32}}{4.5\times 10^{22}} = 5\times 10^{9}\ \text{m}^{-3}$$

10 $$\sigma_n = n_d\, e\mu_n$$

$$\Rightarrow\ 5 = n_d \times 1.6\times 10^{-19}\times 3900$$

$$\therefore\ n_d = \frac{5}{1.6\times 39\times 10^{-17}}$$

$$= 8\times 10^{15} \text{ per cm}^3$$

11 $$I = neAv \text{ or } I \propto nv$$

$$\therefore\ \frac{I_e}{I_h} = \frac{n_e}{n_h}\frac{v_e}{v_h}$$

$$\Rightarrow\ \frac{5}{4} = \frac{n_e}{n_h}\cdot\frac{7}{4}$$

$$\text{or}\ \frac{n_e}{n_h} = \frac{5}{7}$$

12 Current density

$$J = nqv \Rightarrow J_e = n_e\, q\, v_e$$

$$J_h = n_h\, q\, v_h$$

$$\Rightarrow\ \frac{J_e}{J_h} = \frac{n_e}{n_h}\times\frac{v_e}{v_h}$$

$$\frac{3/4}{1/4} = \frac{n_e}{n_h}\times\frac{5}{2} \Rightarrow \frac{n_e}{n_h} = \frac{6}{5}$$

13 Depletion layer is formed due to production of positive ions on *n*-side and negative ions on *p*-side of the junction.

14 In an unbiased *p*-*n* junction, the diffusion of charge carriers across the junction takes place from higher concentration to lower concentration.

15 Barrier potential depends on all the three factor.

16 In forward biasing of *p*-*n* junction, the positive terminal of the battery is connected to *p*-side and the deplection region becomes thin.

17 In the forward biasing of *P*-*N* junction, *p* side of junction diode is connected to higher potential and *n* side of junction diode is connected to lower potential. Hence, the option (a) is correct answer.

18 5V

As it is forward-bias takes +ve value.

19 Here, *p*-*n* junction is reverse biased. Therefore, the current flowing through *p*-*n* junction is zero.

20 Let us assume that current through the diode is *I*.

From the given condition

$$\because\ I = \frac{V_A - V_B}{R} = \frac{4-(-6)}{1\ \text{K}\Omega}$$

$$= \frac{10}{1\times 10^{3}} = 10^{-2}\ \text{A}$$

21 The term LED is abbreviated as Light Emitting Diode. It is forward biased *p* - *n* junction which emits spontaneous radiation. Current in the circuit = 10 mA = 10×10^{-3} A and voltage in the circuit = 6 − 2 = 4V.
From Ohm's law, $V = IR$

$$\Rightarrow\ R = \frac{V}{I} = \frac{4}{10\times 10^{-3}} = 400\ \Omega$$

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22 Band gap, $E = \frac{hc}{\lambda}$

$= \frac{6.6\times 10^{-34}\times 3\times 10^{8}}{2480\times 10^{-9}} \text{J} = \frac{19.8\times 10^{-17}}{2480}$

$= 8\times 10^{-20}\ \text{J} = \frac{8\times 10^{-20}}{1.6\times 10^{-19}} \text{eV}$

$= 5\times 10^{-1} = 0.5$ eV

23 Energy, $E = h\nu = h\frac{c}{\lambda}$

$\Rightarrow \quad \lambda = \frac{hc}{E}$

Substituting the values of h, c and E in the above equation

$\lambda = \frac{6.6\times 10^{-34}\times 3\times 10^{8}}{2.5\times 1.6\times 10^{-19}} = 5000$ Å

As, 4000 Å < 5000 Å

Signal of wavelength 4000 Å can be detected by the photodiode.

24 In a transistor, the base is a conductor of low resistance.

25 To switch ON the transistor, the emitter-base junction of a transistor is forward biased while collector-base junction is reverse biased. The cut-off voltage for silicon is ~1 V, so to switch ON a silicon transistor a potential difference of 1 V approximately, is required between the base and emitter.

26 $\therefore \alpha = \frac{I_C}{I_E} = \frac{I_C}{I_B + I_C}$

$= \frac{0.97}{0.03 + 0.97} = \frac{0.97}{1.00} = 0.97$

27 We have, $R_L = 5000\Omega$, $R_i = 2000\Omega$, $B = 50$

The AC voltage gain is given by

$\beta \times \frac{R_L}{R_i} = \frac{50\times 5000}{2000} = 125$

Thus, the peak output voltage = voltage gain × signal voltage

$= 125 \times 10$ mv

$= 1250$ mV $= 1.25$V

28 Voltage gain in common base amplifier is

$A_v = \alpha \times \frac{R_{\text{out}}}{R_{\text{in}}} = 0.98 \times \frac{400\times 10^{3}}{400}$

$= 980$

$\Rightarrow \quad \alpha = \frac{I_C}{I_E}$

$\therefore I_C = \alpha I_E = 0.98 \times 2\text{ mA} = 1.96\text{ mA}$

$I_E = I_B + I_C \Rightarrow I_B = I_E - I_C = 2\text{ mA} - 1.96\text{ mA} = 0.04\text{ mA}$

29 Base current amplification factor,

$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{2\text{mA}}{40\mu\text{A}} = \frac{2\times 10^{-3}}{40\times 10^{-6}} = 50$

30 Voltage gain, $A_V = \frac{\Delta I_c \times R_L}{\Delta I_b \times R_i}$

$= \frac{(1\times 10^{-3})\times(5\times 10^{-3})}{(15\times 10^{-6})\times 333} \approx 1001$

31 Voltage gain = β × impedance gain

$\Rightarrow \quad 50 = \beta \times \frac{200}{100} \Rightarrow \beta = 25$

Also, power gain = β^2 × impedance gain

$= (25)^2 \times \frac{200}{100} = 1250$

32 Given, collector resistance = $R_{\text{out}} = 2\text{ k}\Omega$

Current amplification factor, $\beta = 100$

Base resistance, $R_{\text{in}} = 1\text{ k}\Omega$

Output signal voltage = 4 V

Putting all the values in given equation, we get

$A_V = \beta\frac{R_{\text{out}}}{R_{\text{in}}} = 100 \times \frac{2\text{ k}\Omega}{1\text{ k}\Omega} \Rightarrow A_V = 200$

Now, $A_V = \frac{(V_{\text{out}})_{\text{AC}}}{(V_{\text{in}})_{\text{AC}}} = 200$

$\Rightarrow \quad (V_{\text{in}})_{\text{AC}} = \frac{4}{200} = 20$ mV

33 Here, $\Delta I_C = 10\times 10^{-3} - 5\times 10^{-3}$

$= 5\times 10^{-3}$ A

$\Delta I_B = 200\times 10^{-6} - 100\times 10^{-6}$

$= 100\times 10^{-6}$A

∴ Current gain,

$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{5}{100} \times 1000 = 50$

34 The symbols given in problem are

(i) OR (ii) AND

(iii) NOT (iv) NAND

35 $Y = \overline{\bar{A}\cdot\bar{B}} = A + B$

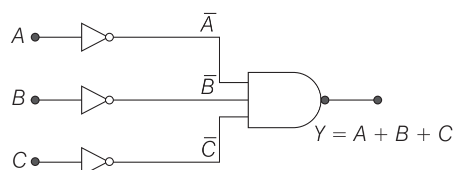
Thus, the combination of the gates produces OR gate.

36

A	*B*	Y_1	Y_2	*Y*
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Above truth table is described AND gate.

37 The simplified circuit is shown in figure below.



So, output $Y = \bar{A}\cdot\bar{B}\cdot\bar{C}$

If $A = 0, B = 1, C = 1$

$\therefore \quad Y = \bar{0}\cdot\bar{1}\cdot\bar{1} = 0 + 1 + 1 = 1$

38 $X = \overline{\overline{AB}} = A\cdot B$ (i.e. AND gate)

If the output X of NAND gate is connected to the input of NOT gate (made from NAND gate by joining two inputs) from the given figure, then we get back an AND gate.

39 We know that, the repetitive use of NAND and NOR gate gives digital circuits.

40 Truth table for given network is

NOR NOR NOT; A, B, Y_1, Y_2, Y

A	B	Y_1	Y_2	Y
0	0	1	0	1
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0

Output Y of network matches with that of NOR gate.

41 Consider the given figure,

The resultant boolean expression of the above logic circuit will be

$Y = (A + B)\cdot C$

Only option (c) is the correct choice, i.e. output $Y = 1$ only when inputs $A = 1$, $B = 0$ and $C = 1$.

42 Output of the given circuit is given by

$y = \overline{(AB)(C)}$

When $A = B = C = 0$,

$Y_1 = \overline{(0)(0)(0)} = \bar{0} = 1$

When $A = B = C = 1$,

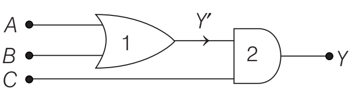
$Y_2 = \overline{(1)(1)} = 0$

43 From the given waveforms, the following truth table can be made

Input		Output
A	*B*	*C*
0	0	0
1	0	1
1	1	1
0	1	1

This truth table is required to OR gate. So, logic circuit gate is OR gate.

44 Gate I is OR gate, $Y' = A + B$



Gate II is AND gate, $Y = Y'\cdot C$

∴ $A = 1, B = 0, C = 1$ will give $Y = 1$

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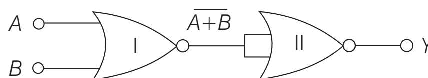
45 We can simplify the gate circuit as



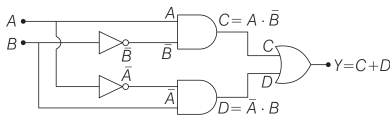
Here, gates I and II are NOR gates. The output $(\overline{A+B})$ of gate I will appear as input of gate II. The final output is

$$Y = \overline{\overline{A + B}} = A + B$$

SESSION 2

1 The Boolean expression which satisfies the output of this logic gate is $C = A \cdot B$, which is for AND gate.

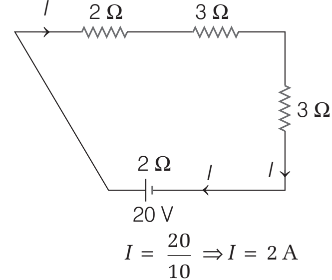
2 According to the question, the figure of combination of gates in terms of inputs and outputs can be given as



Thus, $\quad Y = A \cdot \overline{B} + \overline{A} \cdot B$

3 Due to increase in temperature because of heating, thermal collision between the electron and holes increases. Thus, net electron-hole pairs increase. This leads to increase in the current in diode and overall resistance of the diode changes. This in turn changes both the forward biasing and the reverse biasing. Thus, the overall *I-V* characteristics of *p-n* junction diode gets affected.

4 Since, D_1 is in reverse biased, so current through 5 Ω resistance is zero but D_2 is forward biased, so D_2 behaves as a resistor of zero resistance. The equivalent circuit is



$$I = \frac{20}{10} \Rightarrow I = 2\text{ A}$$

5
$$P = X + \overline{X}Y = X(1 + Y) + \overline{X}Y$$
$$= X + (X + \overline{X})Y$$
$$= X + 1 \cdot Y = X + Y$$

Hence, one gate OR gate.

6 $\therefore \dfrac{N_1}{N_2} = \dfrac{e^{-\Delta E/2kT_1}}{e^{-\Delta E/2kT_2}} = e^{\frac{\Delta E}{2k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$

$$= e^{\frac{1.1\text{eV}}{2 \times 8.62 \times 10^{-5}}\left(\frac{1}{400} - \frac{1}{300}\right)} = e^{-5.31}$$

7 $I = neA(v_e + v_h) = neA(\mu_e + \mu_h)E$

$$= neA(\mu_e + \mu_h)\frac{V}{t}$$
$$= 2 \times 10^{19} \times 1.6 \times 10^{-19} \times 10^{-4} \times (0.33 + 0.17) \times \frac{2.5}{10^{-3}}$$
$$= 0.4\text{ A}$$

8 Solar cell $\rightarrow$ Open circuit $I = 0$, Potential $V = \text{emf}$

$\rightarrow$ Short circuit $I = i$, Potential $V = 0$

9 The four bonding electrons in the case of C lie in the second orbit, whereas in case of Si they lies in the third orbit, so loosely bounded valency electron in Si as compared to C.

$$I_e = I_b + I_c$$

10 We know that a diode only conducts in forward biased condition. In the given circuit, the diode D_1 will be in reverse bias, so it will block the current and diode D_2 will be in forward bias, so it will pass the current

$$i = \frac{V}{R_1 + R_3}$$
$$= \frac{10}{2 + 2} = 2.5\text{ A}$$

11 Input signal of a CE amplifer,

$$V_{\text{in}} = 2\cos\left(15t + \frac{\pi}{3}\right)$$

Voltage gain $A_v = 150$

As CE amplifier gives phase difference of π between input and output signals.

So, $A_v = \dfrac{V_0}{V_{\text{in}}}$

$$\Rightarrow \quad V_0 = A_v V_{\text{in}}$$
$$V_0 = 150 \times 2\cos\left(15t + \frac{\pi}{3} + \pi\right)$$
$$V = 300\cos\left(15t + \frac{4\pi}{3}\right)$$

12 Applying loop law at output port,

$$9 - 4 = I_C R_C$$

or $\quad I_C = 2.5\text{ mA}$

$$I_B = \frac{I_C}{\beta} = \frac{2.5}{90}$$
$$= 2.78 \times 10^{-5}\text{A}$$
$$= 27.8\mu\text{A}$$

Since, the transistor operates in active region, therefore $V_{\text{BE}} = 0.7$ V.

Applying loop law at input port,

$$I_B = \frac{3 - 0.7}{R_B}$$
$$R_B = \frac{2.3 \times 10^5}{2.78}$$
$$= 82\text{ k}\Omega$$

13 As $\quad A_v = \beta\dfrac{R_L}{R_i}$

$$\left[\because g_m = \frac{\Delta I_C}{\Delta V_B} = \frac{\Delta I_C}{\Delta I_B R_i}\right]$$

or $\quad G = \left(\dfrac{\beta}{R_i}\right)R_L \quad \left[\because g_m = \dfrac{\beta}{R_i}\right]$

$\Rightarrow \quad G = g_m R_L$

$\Rightarrow \quad G \propto g_m$

$\therefore \quad \dfrac{G_2}{G_1} = \dfrac{g_{m_1}}{g_{m_2}}$

$\Rightarrow \quad G_2 = \dfrac{0.02}{0.03} \times G$

$\therefore$ Voltage gain, $G_2 = \dfrac{2}{3}G$

14 Current amplification factor, $\beta = \dfrac{\Delta I_C}{\Delta I_B}$

Collector resistance,

$$\Delta I_C = \frac{2V}{2 \times 10^3\ \Omega}$$
$$= 1 \times 10^{-3}\text{A}$$

Base current,

$$\Delta I_B = \frac{V_B}{R_B} = \frac{V_B}{1 \times 10^3} = V_B \times 10^{-3}$$

Given, $\quad \beta = 100$

Now, $\quad 100 = \dfrac{10^{-3}}{V_B \times 10^{-3}}$

$$V_B = \frac{1}{100}\text{V}$$
$$= 10\text{ mV}$$

15 Collector current $i_C = \dfrac{V}{R}$

$$= \frac{3}{3 \times 10^3}$$
$$= 10^{-3}\text{ A}$$

Now base current,

$$i_B = \frac{i_C}{B} = \frac{10^{-3}}{100} = 10^{-5}\text{ A}$$

As, voltage $\quad V_{\text{in}} = i_B R_B$

$\therefore \quad V_{\text{in}} = 10^{-5} \times 2 \times 10^3$

$$= 2 \times 10^{-2}\text{ V}$$

So, voltage gain

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{3}{2 \times 10^{-2}} = 150$$

Power gain $= A_V \times \beta$

$$= 150 \times 100 = 15000$$

16 Given, resistance across load, $R_L = 800\ \Omega$

Voltage drop across load, $V_L = 0.8$ V

Input resistance of circuit, $R_i = 192\ \Omega$.

Collector current is given by,

$$I_C = \frac{V_L}{R_L} = \frac{0.8}{800} = \frac{8}{8000} = 1\text{ mA}$$

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$\because$ Current amplification

$= \frac{\text{Output current}}{\text{Input current}}$

$= \frac{I_C}{I_B} = 0.96$

$\Rightarrow I_B = \frac{1 \text{ mA}}{0.96}$

$\because$ Voltage gain,

$A_V = \frac{V_L}{V_{in}} = \frac{V_L}{I_B R_i}$

$= \frac{0.8 \times 0.96}{10^{-3} \times 192} = 4$

$\Rightarrow \quad A_V = 4$

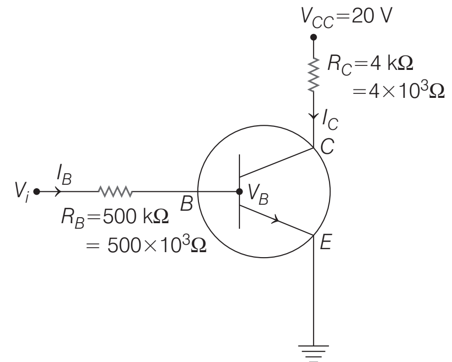
and Power gain,

$A_P = \frac{I_C^2 R_L}{I_B^2 R_i} = \left(\frac{I_C}{I_B}\right)^2 \cdot \frac{R_L}{R_i}$

$= (0.96)^2 \times \frac{800}{192}$

$A_P = 3.84$

17 Given, $V_{BE} = 0$ V, $V_{CE} = 0$ V and $V_i = 20$ V



Applying Kirchhoff's law to the base-emitter loop, we get

$V_i = I_B R_B + V_{BE}$

Substituting the values, we get

$20 = I_B \times (500 \times 10^3) + 0$

$\Rightarrow \quad I_B = \frac{20}{500 \times 10^3} = 0.04 \times 10^{-3}$

$= 40 \times 10^{-6} = 40 \,\mu\text{A} \quad \ldots\text{(i)}$

Similarly, $V_{CC} = I_C R_C + V_{CE}$

Substituting the given values, we get

$20 = I_C \times (4 \times 10^3) + 0$

$\Rightarrow \quad I_C = \frac{20}{4 \times 10^3} = 5 \times 10^{-3} = 5\text{mA} \quad \ldots\text{(ii)}$

Current gain is given as $\beta = \frac{I_C}{I_B}$

Substituting the value of I_B and I_C from Eqs. (i) and (ii), we get

$\Rightarrow \beta = \frac{5 \times 10^{-3}}{40 \times 10^{-6}} = 0.125 \times 10^3 = 125$

18 For using transistor as a switch, it is used in cut-off state and saturation state only.

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